

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):

Robert F. Wallace

Title:

Semiconductor Package Using Terminals Formed on a

Conductive Layer of a Circuit Board

Application No.:

09/866,022

Filing Date:

May 24, 2001

Examiner:

Roy Karl Potter

Group Art Unit:

2822

Docket No.:

SNDK.112US2

Conf. No.:

6172

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR § 1.97(b)

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying form PTO-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed.

Citation of these documents shall not be construed as:

- 1. an admission that the documents are necessarily prior art with respect to the instant invention;
- 2. a representation that a search has been made, a representation that a search has been made, (other than as indicated by any cited document); or

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Attorney Docket No.: SNDK.112US2

Application No.: 09/866,022

3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

Certificate of Mailing Under 37 CFR 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope address to:

Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 24, 2004.

Franklip Dyer

Respectfully submitted,

Gerald P. Parsons

Reg. No. 24,486

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U.S. Departme	ent of Co	mmerce, Patent and		Atty Docket No.					
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)					Applicant Robert. F. Wallace				
									
					May ****, 2001		Unassigned		
					*Examination	- Arta		U.S.	Patent Documents
*Examile AAD Initial		Document Number	Date	Name	Class	Subclass	Filing I		
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Examiner	•		Date Consider	ed	•••				
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